Design and Implementation of Photovoltaic Single Stage Inverter Connected to Grid

Bayu Prasetyo[1], Mochamad Ashari[1], and Dedet C. Riawan[1]

Abstract— ***Photovoltaic system that connected to grid is a system which applied for an area that can be reach by transmission line. This system as a support for conventional generating system. If there is a power from PV system, then power demand supplied from photovoltaic generating system. Otherwise, power demand supplied from conventional generating system. As a support conventional generating system, there is many methods to convert photo energy into AC system that connected to grid. One of conventional methods as a two stage inverter, this methods need two process to convert photovoltaic into AC system. First stage, conversion photovoltaic power to DC system. In this stage, PV processed by buck boost converter. Second stage, that DC power from first stage changed into AC power system. This two stage process has low efficiency, so we try to make the process simply and more efficiency. New method called single stage inverter can be applied. With this methods, conversion DC power system from PV can be done by single stage process. From this single process, we expext that more efficiency can be achieved.***

Keywords— Photovoltaic, Inverter, Grid Connected.

I. INTRODUCTION

HIGH initial investment and limited life span of a photovoltaic (PV) array makes it necessary for the user to extract maximum power from the PV system. The nonlinear i–v characteristics of the PV array [1] and the rotation and revolution of the earth around the sun, further necessitate the application of maximum power point tracking (MPPT) [2] to the system. In this context, grid connected PV systems have become very popular because they do not need battery back-ups to ensure MPPT. Standalone systems can also achieve MPPT, but They would need suitable battery back-ups for this purpose.

Though, multistage systems [1] have been reported for certain applications, grid connected PV systems usually employ two stages [Figure. 1(a)] to appropriately condition the available solar power for feeding into the grid. While the first stage is used to boost the PV array voltage and track the maximum solar power, the second stage inverts this dc power into high quality ac power. Typically, the first stage comprises of a boost or buck-boost type dc–dc converter topology. Such two-stage configurations are time tested and work well, but have drawbacks such as higher part count, lower efficiency, lower reliability, higher cost and larger size. The question is whether it is possible to reduce the number of power processing stages in such systems or, in short, is it possible to realize the situation depicted in Figure. 1(b). Two simple and straightforward solutions to this requirement could be as follows.

1. Using the conventional H-bridge inverter followed by a step-up transformer [3].
2. Using an array with sufficiently large PV voltage, which may be realized using a string of series connected modules followed by an H-bridge inverter [4], [5].

While these options are feasible, they suffer from the following drawbacks. Adding a transformer (corresponding to the grid frequency) will add to the bulk and cost of the system, besides adding losses. On the other hand, a PV array with large dc voltage suffers from drawbacks such as hot-spots during partial shading of the array, reduced safety and increased probability of leakage current through the parasitic capacitance between the panel and the system ground. Further, in both the options, the inverter must take care of the MPPT.

In view of the ongoing discussion, it is reasonable to conclude that the best option is to have only a single power electronic stage between the PV array and the grid to achieve all the functions—namely the electrical MPPT, boosting and inversion [Figure. 1(b)] leading to a compact system. Such compact systems are also in line with the modern day need to have highly integrated systems built into modules having high reliability, high performance (e.g., intelligence, protection, low electromagnetic interference (EMI), etc.), reduced weight and low cost. Lesser is the number of (power) stages, easier is the module integration. Also, the number of devices in a power stage should also be minimized. In other words, a complete circuit optimization is required.

A survey conducted by the authors revealed that limited literature is available related to single-stage, grid connected PV systems. There are some other configurations [7]–[9] which are not originally intended for PV applications, but can be considered for grid connected PV applications. Some of these topologies are briefly discussed in Section II of this paper.

This paper proposes a new single-stage configuration, suitable for grid connected PV or standalone applications. Salient features of the proposed configuration are summarized as follows.

1. Better utilization of the available PV source compared to the topology proposed by Kasa *et al*.
2. Proposed topology is simple, symmetrical and requires a simple sine triangle PWM control for its operation and maximum power point tracking of the PV source.
3. As the number of power devices is optimal, the system is reliable, efficient and economical.
4. Due to the very nature of the proposed topology, the PV source appears floating to the grid. This eliminates the requirement of a transformer for safety

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and grounding. A local earth, created for the grounding of the PV array, will suffice.

5. Optimal switching and conduction losses, in addition to the optimal utilization of switching devices, result in low losses and hence low cooling requirements. Only one device at a time is switched at high frequency, reducing the EMI concerns. Also number of devices conducting during any mode is optimum, resulting in minimum conduction losses apart from lowering the cost.
6. Power handling capacity of the proposed configuration is higher because for each half cycle of the grid voltage, there is a separate, dedicated inductor and switch to handle the power. Also, there are no coupled inductors or flyback transformer in the circuit for intermediate power transfer [9], [10].

II. Survey of Single-Stage Topologies Suitablefor Grid Connected Pv Systems

Caceres and Barbi [6] have proposed an elegant single-stage boost cum inverter topology [Figure. 2] having two boost converters operating in a complementary manner. Though, not specifically intended for PV applications, this circuit is a good candidate for a single-stage, compact grid connected PV application. However, the topology suffers from the following drawbacks. All the devices are simultaneously hard switched at high frequency, rendering the system prone to EMI problems and causing more switching losses.

Another topology, derived from the basic Zeta and Cuk configuration, has been proposed by Schekulin and is shown in Figure. 3. This is an improved configuration as it uses minima lnumber of devices and does not have the drawbacks of simultaneous, high frequency operation of all the switching devices. In the positive half cycle of the grid voltage, S1 operates at high frequency while S2 and S4 are kept ON. Power transfer during this period is based on the buck-boost principle. Similarly, during the negative half cycle, S2 is operated at high frequency while S1and S3 are kept continuously ON. Power transfer during this period follows the boost principle as source is active during both the ON and OFF intervals. This leads to asymmetrical operation of the converter in the two halves of the grid cycle, which is a major drawback of this system because it necessitates an appropriate(and probably complex) control strategy to prevent dc current injection into the grid. The main advantage of this configuration is that it has low switching losses.

Another topology proposed by Kasa *et al.*, [6], is based on a half-bridge buck-boost inverter configuration, as shown in Figure. 4. This configuration eliminates the drawback of asymmetrical operation during the two half cycles of a grid voltage. Again, it is a good configuration as it has minimum switching and conduction losses because only two devices are used during any half cycle of the grid voltage. Since a minimum number of switches are operated at high frequency so it has less EMI concerns and high reliability. The drawbacks with this configuration, however, are that it uses a pair of PV sources only one of which is utilized in a given half cycle of the grid voltage. High value of filter capacitor across each of these PV sources is required.

Kasa *et al.* have also proposed an isolated, flyback configuration [Figure.5] which is a modification of the half bridge buck- boost topology shown in Figure.4. This topology uses only three power devices and an isolation transformer. It also uses the buck-boost principle [6]. This is a good scheme, but is applicable to low power systems only, typically less than 500W,due to the limitation on the value of primary inductance of the flyback transformer. Also, there are additional losses duet o the transformer, though it provides isolation between the PV and grid sides.

Wang [8] has proposed a single-stage, full bridge configuration based on the buck-boost principle as shown in Figure. 6.During the positive half cycle of the grid voltage, S4 operates at high frequency and S1 is kept continuously ON. The path during turn OFF is completed through S1 and D2. During the negative half cycle of the grid voltage, S3 operates at high frequency and S2 is kept continuously ON. During turn OFF, the path is completed through S2 and D1. This configuration has a large number of devices conducting at a given instant resulting in higher conduction losses.

Based on the buck-boost principle, Xue *et al.* have proposed yet another single-stage grid connected PV system, as shown in Figure.7. Proposed configuration uses flyback principle with mutually coupled coils during the negative half cycle of the grid voltage. The limitation of this system is that it can be used only for low power applications due to the limitation of the mutually coupled coils or flyback transformer to handle high power [11]. In addition to this, the switching and conduction losses are higher and the operation is asymmetrical in the two halves of the grid voltage cycle.

Wang [9] has proposed another single-stage configuration based on buck-boost principle as shown in Figure.8. Though this configuration is not specifically intended for grid connected PV systems, it may be considered for this application. But the drawback with this configuration is that it uses five switches, with three switches operating at high frequency, leading to EMI concerns and higher switching losses.

Huang *et al.* have proposed a single stage configuration for a split–phase system for PV applications, which uses a -source inverter. This configuration, which requires six switches, operating at high frequency, is recommended for high power applications.

This paper proposes a single stage topology based on buck boost principle as shown in Figure.9. During the positive half cycle of the grid voltage, operates at high frequency while is kept continuously ON. During the negative half cycle, is operated at high frequency while is kept continuously ON. As an optimum number of switches are operated at any given time, the proposed topology has the advantage of low switching and conduction losses, low EMI and low cooling requirements. The proposed topology overcomes several drawbacks of the topologies surveyed and described in this section. Working principle and all other details of this topology are presented in the following section.

III. Proposed Topology

The proposed topology consists of two dc-to-dc, buck-boost converters connected as shown in Figure 10. Each of these converters operates in DCM for one half cycle

of the fundamental grid voltage. The resulting circuit acts as a current source inverter which feeds sinusoidal current into a low value capacitor across the grid. DCM operation helps in feeding sinusoidal current with near unity power factor (UPF) into the grid because the energy can be drawn in the form of "energy packets" whose magnitudes vary in a sinusoidal manner.

The power device SWp1 (or SWn1) is switched at high frequency whileSWp2 (or SWn2) is kept continuously ON during the positive half cycle (or negative half cycle). SWp1 (or SWn1)is switched as per sine triangle pulse width modulation(SPWM) method. When is SWp1 ON, energy is stored in the buck-boost inductor "LBB" by the PV source. When SWp1 is OFF, Dp (or Dn) gets forward biased, discharging the stored inductor energy into capacitor Cf which feeds sinusoidal current into the grid. The state equations governing the operation of the proposed configuration during the positive half cycle of the grid voltage are given below. The switching control strategy implemented is also shown in Figure. 11.

When power device is ON. Applying KCL to the nodes "a" and "e" and KVL to the loops a-b-c-d-a and e-f-g-h-e, the following state equations are obtained:

$$i_{pv} = C_p\, x'_1 + x_{2p}; \quad C_f\, x'_3 + x_4 = 0;$$
$$x_1 = L_{BB}\, x'_{2p}; \quad x_3 = L_f\, x'_4 + v_{ac}. \qquad (1)$$

When power device is OFF, and diode is conducting. Applying KCL to the nodes "a" and "e" and KVL to the loops j-b-e-h-i-j and e-f-g-h-e, yields the following state equations:

$$i_{pv} = C_p\, x'_1; \quad C_f\, x'_3 + x_4 = x_{2p};$$
$$-x_3 = L_{BB}\, x'_{2p}; \quad x_3 = L_f\, x'_4 + v_{ac}. \qquad (2)$$

When power device is OFF, and diode is not conducting. Applying KCL to the nodes "a" and "e" and KVL to the loop e-f-g-h-e, results in the following state equations:

$$i_{pv} = C_p\, x'_1; \quad C_f\, x'_3 + x_4 = 0;$$
$$0 = L_{BB}\, x'_{2p}; \quad x_3 = (L_f)\, x'_4 + v_{ac}. \qquad (3)$$

In a similar manner, state space equations can be written for negative cycle when other half of the inverter is operated. Using these state space equations, the complete PV system is simulated in MATLAB/SIMULINK software [12].

For analysis of the proposed configuration, the following assumptions are made.

1. Switching frequency is 2n times the fundamental frequency of the grid voltage.
2. Grid voltage is constant over a high frequency switching time period.
3. Value of duty cycle is constant over a high frequency switching time period.
4. DCM operation during the entire cycle of the grid voltage.
5. The PV array followed by 'C_p' provides a dc voltage V_{pv} which is constant over the entire grid cycle.

In view of assumption (1) , one complete cycle of grid voltage can be divided into *2n* high switching periods.

IV. Design and Implementation

From the Figure 10 and Figure 11, now we can design a simulation and calculate the component that build a single stage inverter.

From Figure 12, we calculate component inductor L_{BB1} and L_{BB2},inductor L_f, Capasitor C_f, and Capasitor C_p. Inverter operated in Continous Conduction Mode (CCM). Basic parameter that use to design assume :

a. PV maximum power (P_{max}) :1440 W
b. PV voltageat P_{max} (V_{pv}) :205.2 V
c. Voltage peak at grid (V_{gm}) :311V
d. Switching maximum frequency (f_{smax}) :30 KHz
e. Amplitudo max reference current (A) :100 A
f. Limit reference current (ΔI) :10 A
g. Voltage ripple grid maximum (ΔV_g) :50 V
h. Frekuensi Cutoff (f_c) :1 KHz
i. Frekuensi Grid (f_g) :50 Hz
j. Voltage ripple PV maximum (ΔV) :5 V

A. Design Inductor L_{BB}

The buck-boost inductor, 'L_{BB}' acts as an energy storage element, which stores energy from the PV source and transfers it to the grid through capacitor C_f. The maximum energy is transferred during the peak interval, when PV is delivering rated power "*P* " W.

$$L_{BB} = \frac{1}{f_{s(\max)} \times 2 \times \Delta I} \times \left(\frac{1}{V_{PV}} \times \frac{1}{V_{gm}}\right)^{-1} \qquad (4)$$

$$L_{BB} = \frac{1}{30.10^3 \times 2 \times 10} \times \left(\frac{1}{205.2} \times \frac{1}{311}\right)^{-1} = 0.2\ mH$$

B. Design Capasitor C_f

For designing Capasitor C_f we need maximum energy that transferred by inductor L_{BB}. If V is voltage that pass the capasitor C, so energy that saved is :

$$(e) = 0.5\ x\ C\ x\ V^2 \qquad (5)$$

If we assume that power factor = 1, then energy maximum that transferred is a grid voltage peak. As long as OFF period in inverter switch, the decrease energy in inductor L_{BB} equal to increase energy that saved in the Capasitor C_f . So, we can calculate that C_f that we use :

$$C_f = \frac{L_{BB} \times A \times \Delta I}{V_{gm} \times \Delta V} \qquad (6)$$

$$L_{BB} = \frac{0.2.10^{-3} \times 100 \times 10}{311 \times 50} = 13\ \mu F$$

C. Design Inductor L_f

L_f is the filter inductor which filters the high switching frequency component present in the current waveform fed into the grid. For design, it requires the cut off frequency (f_c) to be lesser than the switching frequency. Thus, the design value of L_f is given by

$$L_f = \frac{1}{(2 \times \pi \times f_c)^2 \times C_f}. \qquad (7)$$

$$L_{BB} = \frac{1}{(2 \times 3.14 \times 1000)^2 \times 13.10^{-6}} = 2\ mH$$

D. Design Capasitor C_p

C_p acts as a buffer between the PV source and the proposed inverter configuration. Value of C_p decides the maximum amplitude of ripple in the voltage of the PV array. Let Δ_{vPV} be the maximum value of the allowed ripple in the PV voltage and f_g be the frequency of the fundamental cycle of the grid voltage, then the design value of C_p is given by[8].

$$C_p = \frac{2 \times P}{4 \times (2 \times \pi \times f_g) \times V_{PV} \times \Delta_{vPV}}. \qquad (8)$$

$$C_p = \frac{2 \times 1440}{4 \times 2 \times 3.14 \times 50 \times 205.2 \times 5} = 2.2mF$$

E. Simulation

In this simulation result, will show about simulation that have been made in PSIM software.

From Figure 13, we know that pulse from probe V_1 and V_2 follow the frequency from grid and always inverting one to each other. In this case, we can use Zero Crossing Detector (ZCD). ZCD applied by comparing signal grid with ground. After we get ZCD signal, we can inverting this signal to get complementary work of the signal. Finally, this two signal that get from ZCD (also inverting signal) used to trigger S_{p2} and S_{n2} (see Figure 12).

Probe V_3 and $V_{4\ has}$ SPWM output. This SPWM can get by compare sinusoidal pulse (which can get from grid) and triangle pulse (carrier pulse). As we see, V_3 and V_4 also inverting one to each other. Because we need S_{p1} and S_{n1} work complementary, so the sinusoidal signal that we can get from grid, invert by phase inverting (that we can make it by op-amp).

From the simulation, we can increase grid power (W) by manipulating SPWM in S_{p1} and S_{n1}. We can modulate the amplitude of grid signal by voltage divider (in next chapter). Actually we can also modulate the amplitude carrier frequency, but this way will take a risk of frequency change due to amplitude change.

However, the grid voltage was found to have some distortion. Hence, the grid voltage must be filtered to obtain the fundamental component. Hence, the generation of sine wave (used in SPWM) is done by attenuating the sensed grid voltage and then passing it through a 'lowpass' filter to render a unit amplitude pure sinewave. This wave form is then passed through an'all-pass' filter to compensate for any phase shift.

From Figure 15, we know that V_{grid} and I_L have same phase. In sinusoidal form we can ensure that inverter can connect to the grid because the same phase between inverter and grid.

From Figure 16, Buck Boost Inductor current presented. That shows process charging and discharging in inductor L_{BB}.

F. Hardware Implementation

From Figure.17, we can get 3 main basic function: phase inverting, Zero Crossing Detector (ZCD), and comparator. First, transformator that connect to grid acts as clock for this system. The AC 220 V sides step down to the AC 4.5 V, to get connect to other component. This 4.5 V_{AC} connect to variable resistor, it make voltage divider circuit. By the voltage divider circuit, we can adjust the amplitude of 4.5 V_{AC} before in the phase inverting and Zero Crossing Detector circuit. As mention before in simulation, we can change the power that we want to deliver out from inverter side by modulating the amplitude.

This phase inverting use LM 741 which known as general purpose operational amplifier. Here we use gain about -1 to get phase output inverted from phase input. With gain -1, signal input doesn't multiply the amplitude, just invert it. Dual supply are used to operate this operational amplifier. As we need the inverting output, then we put signal input to the inverting input pin and non inverting input we connect it to ground.

From Figure 19, we know how phase inverting schematic applied. It shows sinusoidal signal grid inverted when we take signal at pin 6 of LM741. Signal output from LM 741 always complementary with the signal grid. At next, This signal will compare with signal triangle to get Sinusoidal PWM (SPWM).

For Zero Crossing Detector (ZCD), we use LM 339 which known as comparator. For ZCD, we don't need any gain for the input signal, just make the square output which have same frequency with the grid. In datasheet LM 339 showed that for configurating LM 339 as a ZCD we need dual supply voltage. Signal input given at non inverting input pin, and inverting input connected to ground.

Due to the dual supply voltage, output from ZCD have positive area (0 and +12v) and negative area (0 and -12v). So we add the diode (Figure 22) at the output of comparator. Dioda will pass the signal in positive area and blocked the signal in negative area. Pull up resistor use to fix output signal due to output impedance.

To trigger swiching devices (FET) we need 2 ZCD pulse output that work complementary. So we add the inverting phase schematic in the ZCD. It makes ZCD has 2 output that works complementary.

At the carrier signal, we use XR 2206 which configure as triangle pulse generator. With this schematic, we can change frequency by manipulating R and C at pin 5, 6, and 7. To change the amplitude, we can varying the variable resistor at pin 3. The use of XR 2206 is more simply than we use Timer IC 555 which fix designed to generate pulse.

V. CONCLUSION

In this work, the importance of single-stage grid connected PV systems has been highlighted. A single stage topology with improved features has been proposed. Relevant analysis, including derivations of the expressions for peak voltage and current stresses across the switching devices, has been performed and a design procedure has been presented. The topology is simple, symmetrical and easy to control. The other desirable features include good efficiency due to optimal number of device switchings and reduced switching losses. A comparison of the proposed configuration with several existing configurations.

The diodes (Dp and Dn), which a reinherent to the buck-boost operation, also serve to prevent any reverse power flow from the power grid to the PV array. DCM operation ensures better control a part from facilitating the generation and feeding of high quality current into the grid. DCM operation also eliminates the requirement of fast recovery diodes (i.e Dp and Dn).Thus, the design of the buck boost inductor is crucial , since the system must operate in DCM under any operating condition.

Proposed configuration is highly suitable for an integrated solution (e.g.,plug-and-play type ac modules) for PV systems. In this work, MOSFETs are used as switching devices. If low loss devices, like IGBTs, are used the efficiency can be further improved.

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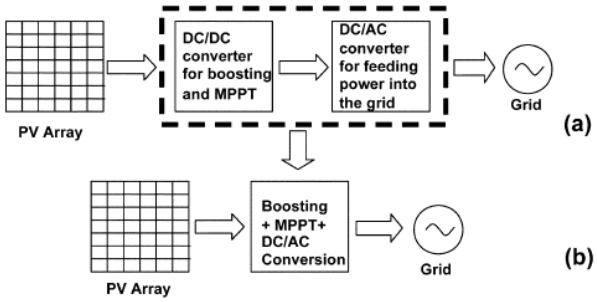


Figure 1.Grid connected PV system topologies:(a)conventional two-stage and (b)single-stage configuration

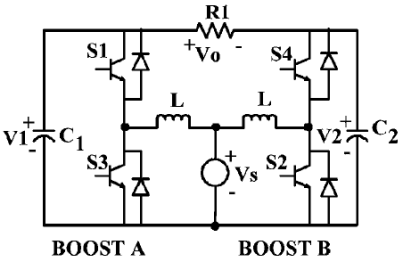


Figure 2. topology proposed by *Caceres and Barbi*

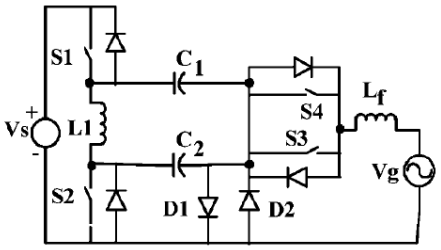


Figure 3. topology proposed by Schekulin

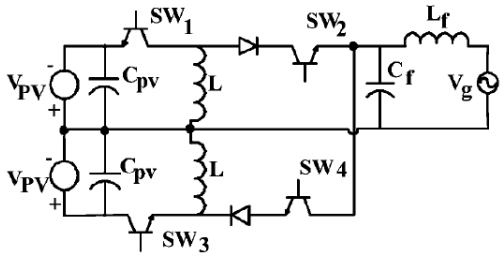


Figure 4. topology proposed by Kasa

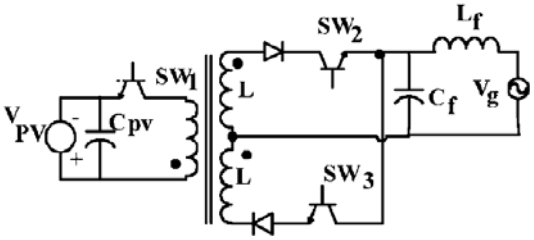


Figure 5. topology proposed by Kasa (flyback configuration)

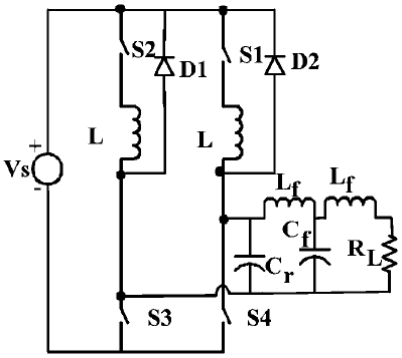


Figure 6. topology proposed by Wang

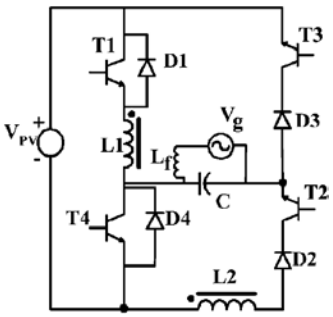


Figure 7. topology proposed by Xue

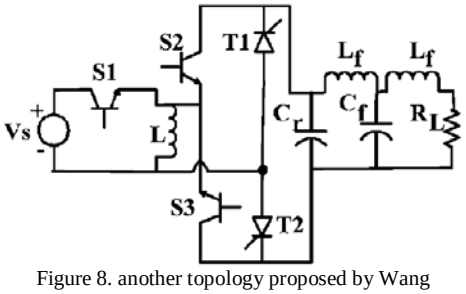


Figure 8. another topology proposed by Wang

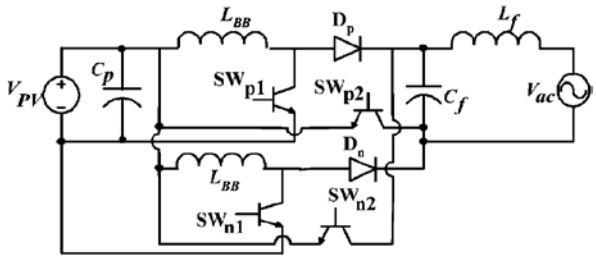


Figure 9. proposed scheme

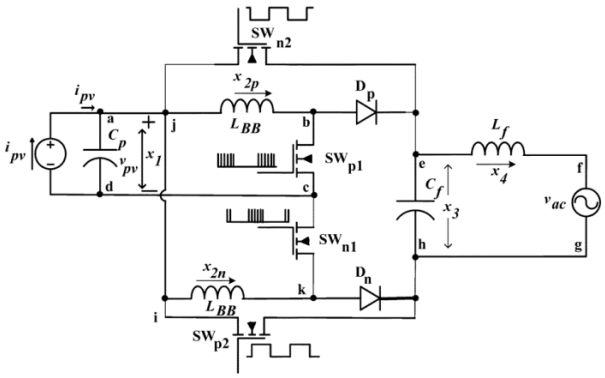


Figure 10. Complete schematic diagram of the proposed single-stage grid connected PV

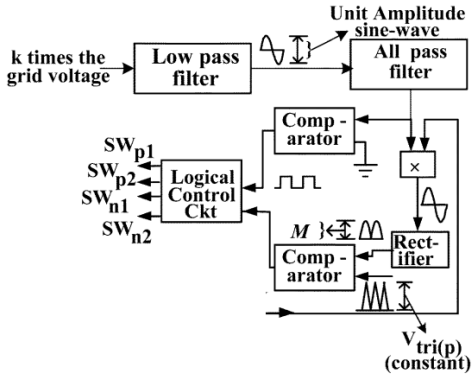
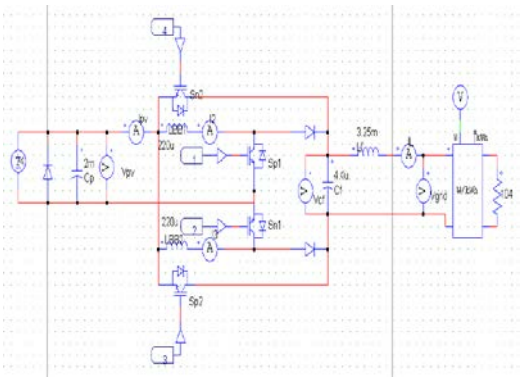


Figure 11. Control Strategy



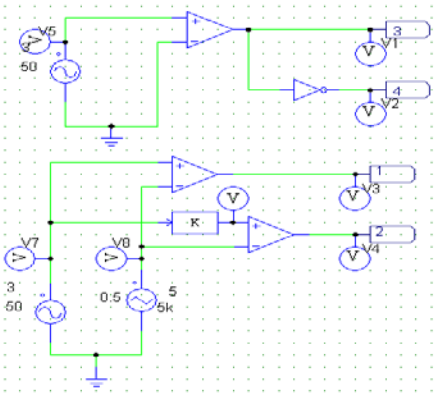


Figure 12. Simulation design of single-stagegrid connected PV

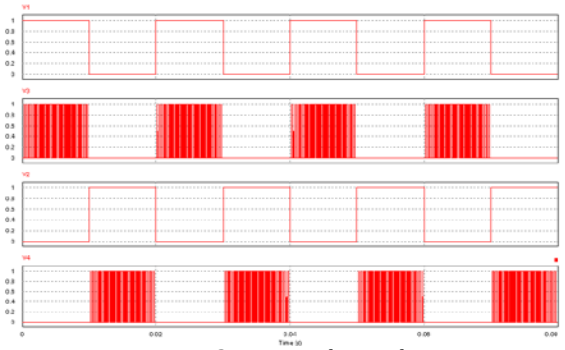


Figure 13. Trigger pulse simulation

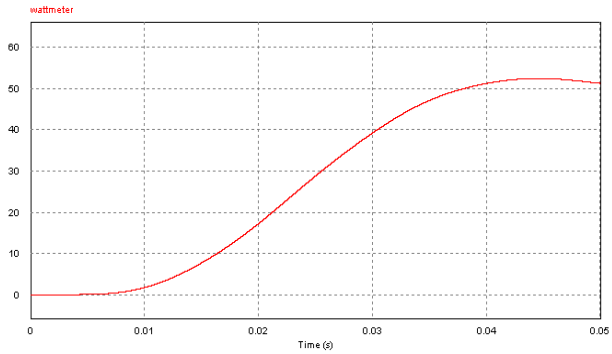
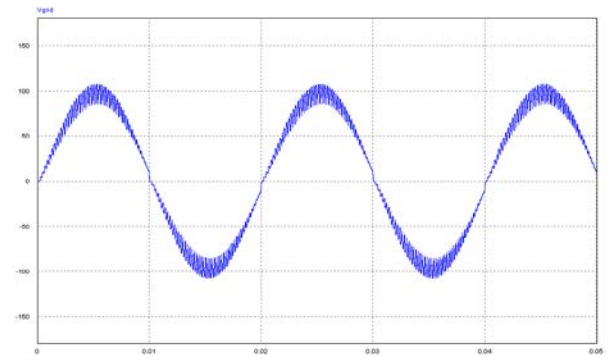


Figure 14. Wattmeter simulation



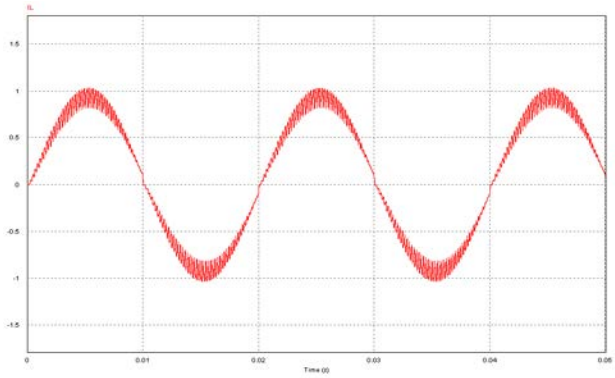


Figure 15. V grid and IL Simulation

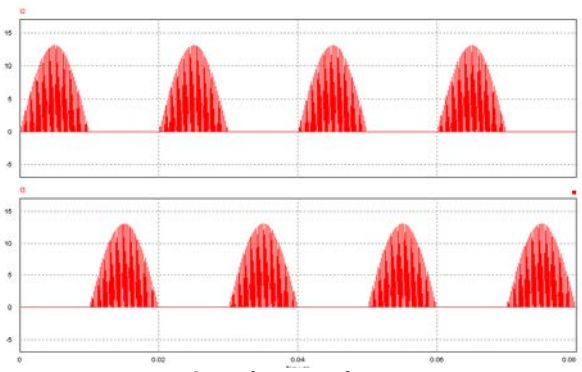


Figure 16. Buck Boost Inductor current

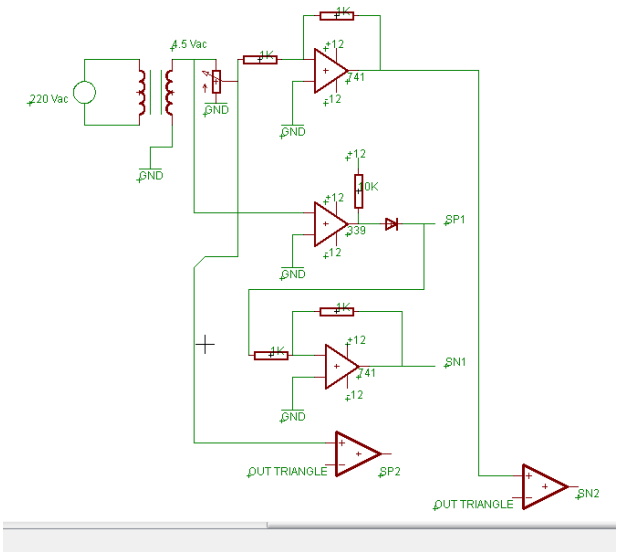


Figure 17. Triggering schematic

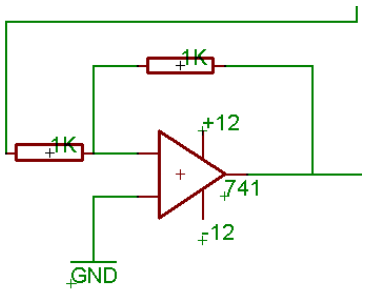


Figure 18. Phase inverting schematic

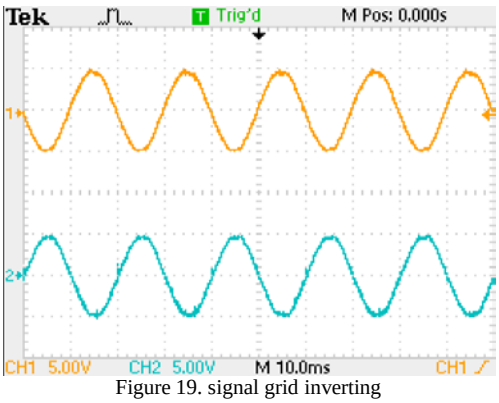


Figure 19. signal grid inverting

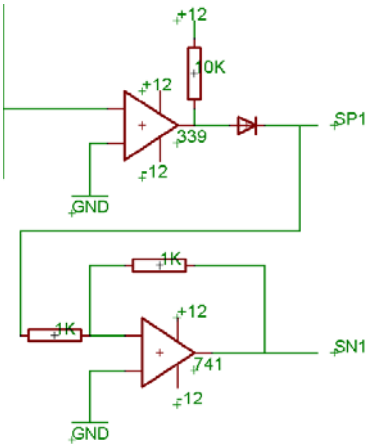


Figure 20. Zero Crossing detector and phase inverting schematic

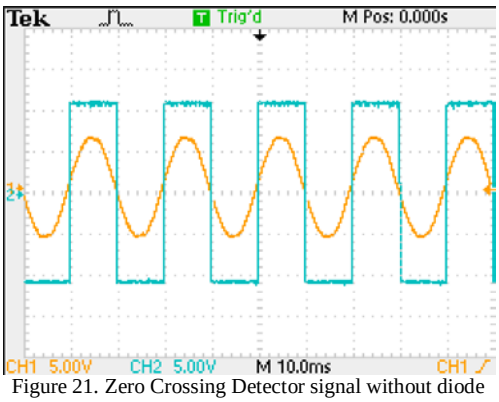


Figure 21. Zero Crossing Detector signal without diode

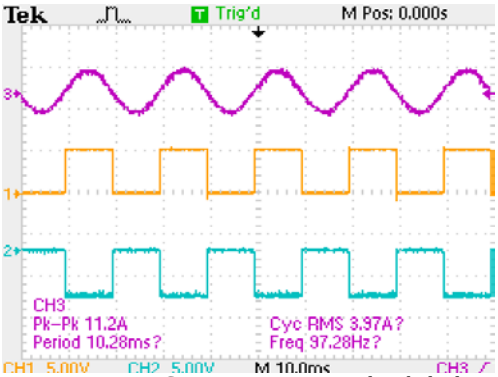


Figure 22. Zero Crossing Detector signal with diode

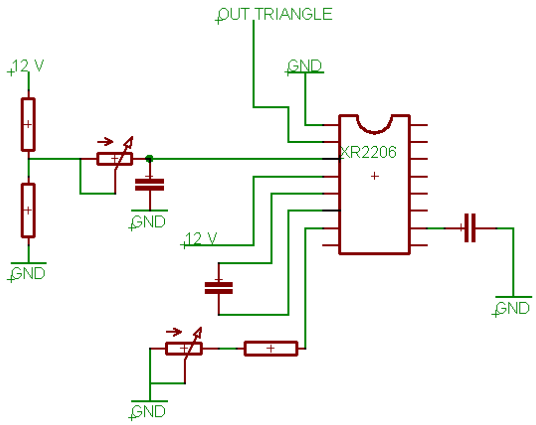


Figure 23. XR 2206 configuration schematic

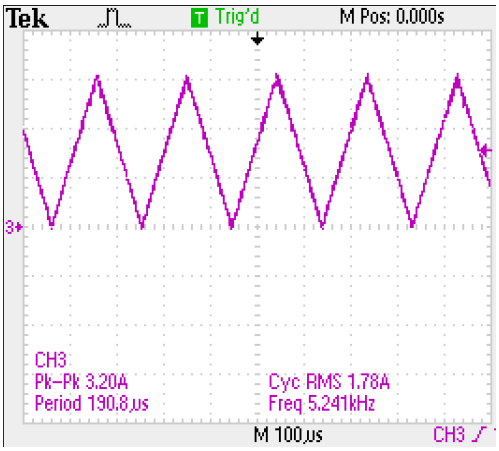


Figure 24. Carrier Signal

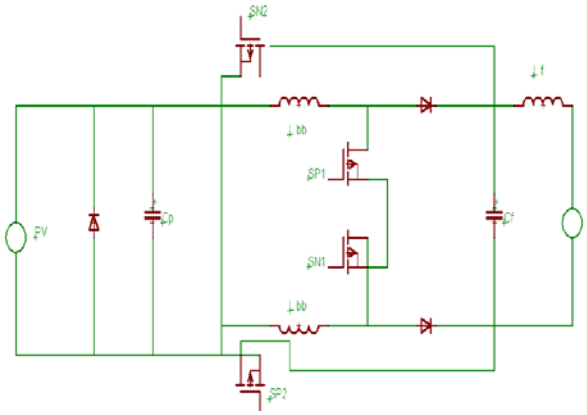


Figure 25. Buck boost inverter schematic

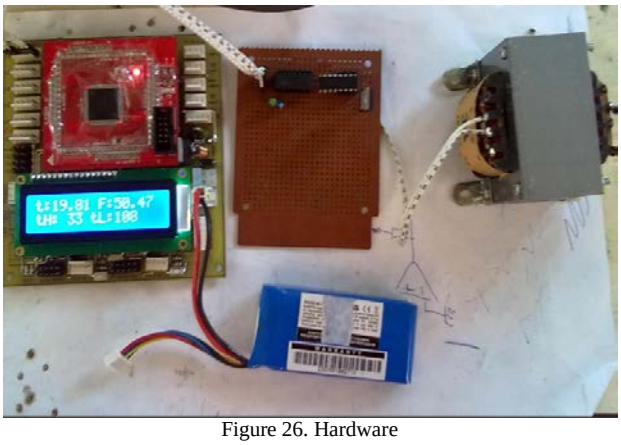


Figure 26. Hardware